Designing with Xilinx Serial Transceivers

Connectivity 3

CONN-TRX-ILT (v1.0)

Course Specification

Course Description

In this two-day course, you will learn how to employ serial transceivers in your 7 series or UltraScale™ FPGA or MPSoC design. You will identify and use the features of the serial transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection.

Additional topics include use of the Transceivers Wizards, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

Level – Connectivity 3

Course Duration – 2 days

Price – $1800 or 18 Xilinx Training Credits

Course Part Number – CONN-TRX-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Designing with Verilog or the Designing with VHDL
- Designing FPGAs Using the Vivado Design Suite 1
- Designing FPGAs Using the Vivado Design Suite 2
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Vivado® System Edition 2016.3
- Mentor Graphics Questa Advanced Simulator 10.4

Hardware

- Architecture: 7 series and UltraScale FPGAs
- Demo board: Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 board*

* This course focuses on the UltraScale and 7 series architectures. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe and use the ports and attributes of the serial transceivers in Xilinx FPGAs and MPSoCs
- Effectively use the following features of the gigabit transceivers:
  - 64B/66B and other encoding/decoding, comma detection, clock correction, and channel bonding
  - Pre-emphasis and receive equalization
- Use the Transceivers Wizards to instantiate GT primitives in a design
- Access appropriate reference material for board design issues involving signal integrity and the power supply, reference clocking, and trace design
- Use the IBERT design to verify transceiver links on real hardware

Course Outline

Day 1

- 7 Series and UltraScale Transceivers Overview
- 7 Series and UltraScale Transceivers Clocking and Resets
- Transceiver IP Generation – Transceiver Wizard
- **Lab 1:** Transceiver Core Generation
- Transceiver Simulation
- **Lab 2:** Transceiver Simulation
- PCS Layer General Functionality
- PCS Layer Encoding
- **Lab 3:** 64B/66B Encoding

Day 2

- Transceiver Implementation
- **Lab 4**: Transceiver Implementation
- PMA Layer Details
- PMA Layer Optimization
- **Lab 5**: IBERT Design
- Transceiver Test and Debugging
- **Lab 6**: Transceiver Debugging
- Transceiver Board Design Considerations
- Transceiver Application Examples

Lab Descriptions

- **Lab 1:** Transceiver Core Generation – Use the Transceivers Wizard to create instantiation templates.
- **Lab 2:** Transceiver Simulation – Simulate the transceiver IP by using the IP example design.
- **Lab 3:** 64B/66B Encoding – Generate a 64B/66B transceiver core by using the Transceivers Wizard, simulate the design, and analyze the results.
- **Lab 4:** Transceiver Implementation – Implement the transceiver IP by using the IP example design.
- **Lab 5:** IBERT Design – Verify transceiver links on real hardware.
- **Lab 6:** Transceiver Debugging – Debug transceiver links.

Register Today

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