Essential DSP Implementation Techniques

DSP 3

DSP-ESS-ILT (v1.0)

Course Specification

Course Description

This course provides a foundation for Digital Signal Processing (DSP) techniques for Xilinx FPGAs. The course begins with a refresher of basic binary number theory, mathematics, and the essential features within the FPGA that are important to signal processing. The body of the course explores a variety of filter techniques with emphasis on optimal implementation in Xilinx devices and continues with an examination of FFTs, video, and image processing. Throughout the course, Xilinx cores and IP relevant to signal processing are introduced. The course is complemented by hands-on exercises to reinforce the concepts learned.

Level – DSP 3

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – DSP-ESS-ILT

Who Should Attend? – Engineers and designers who have an interest in developing products that use digital signal processing

Prerequisites

A fundamental understanding of digital signal processing theory, including an understanding of the following principles:

- Sample rates
- Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters
- Oscillators and mixers
- Fast Fourier Transform (FFT) algorithm

Recommended

- Designing FPGAs Using the Vivado Design Suite 1

Follow-up courses

- C-based Design: High-Level Synthesis with the Vivado HLx Tool
- DSP Design Using System Generator
- Embedded C/C++ Development Environment and Methodology

Hardware

- Architecture: 7 series FPGAs*
- Demo board: None*

* This course focuses on the 7 series FPGA architecture. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the advantages of using FPGAs over traditional processors for DSP designs
- Utilize fixed point binary arithmetic and identify how to use this knowledge to create efficient designs in FPGAs
- Recognize how both the CLB slices in FPGAs and the more advanced DSP48s are used to implement DSP algorithms
- Explain the dataflow through the device and how to use distributed memory, block RAM, registers, and SRLs to properly implement these designs
- Construct different FIR filter and FFT implementations and how to optimize these implementations in the FPGA
- Explain the algorithms for video and imaging systems and their implementations in FPGAs

Course Outline

Day 1

- Back to Basics
- Architecture
- FPGA Math
- **Exercise 1:** Signed Number Conversion, Quantization and Rounding, Adders, Subtractors, and Accumulation
- Shift Registers, RAM, and Applications
- **Exercise 2:** SRL32E and RAM Estimation and Concatenation
- FIR Filter
- **Exercise 3:** Filter Implementation, Resource and Performance Estimation

Day 2

- Advanced Filter Techniques
- **Exercise 4:** Filter Implementations, Resource and Performance Estimation
- Fast Fourier Transform
- **Exercise 5:** FFT Implementation, Resource and Performance Estimation
- Video and Imaging
- Where Do We Go From Here?
- **Demonstration:** System Generator and the CORE Generator Tool with a DSP-Targeted Reference Design
- Where Can I Learn More?

Lab Descriptions

- **Exercise 1:** Signed Number Conversion, Quantization and Rounding, Adders, Subtractors, and Accumulation – Learn how to estimate device resource utilization for basic math functions. Compare different methodologies for implementing functions.
- **Exercise 2:** SRL32E and RAM Estimation and Concatenation – Learn how to optimize memory and storage in Xilinx FPGAs.
- **Exercise 3:** Filter Implementation, Resource and Performance Estimation – Learn how and when to use various implementation strategies for optimal filter implementation.
- **Exercise 4:** Filter Implementations, Resource and Performance Estimation – Advanced filter topologies are studied. Architect multichannel and multirate filters using various methods. Implementation strategies will be discussed and optimal methods used.
- **Exercise 5:** FFT Implementation, Resource and Performance Estimation – Select correct parameters for FFT implementations to meet design targets. Resource estimation will be studied and trade-offs with performance examined through implementation examples.
- **Demonstration:** System Generator and the CORE Generator Tool with a DSP-Targeted Reference Design – Introduces DSP-targeted hardware boards and software tools. Witness the power, ease of use, and design efficiency of Xilinx DSP tools and IP. Reinforce the concepts studied in the course material and exercises.

Register Today

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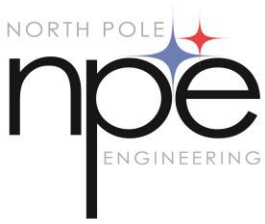

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.