Zynq Master Training for Experienced FPGA Engineers

Embedded Architect 3

EMBD-33040-ILT (v1.0)

Course Specification

Course Description

The Xilinx Zynq® All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course provides system architects with the knowledge to effectively architect a Zynq All Programmable SoC and/or MicroBlaze using IP Integrator (IPI) and troubleshooting from hardware and software concurrently using Vivado Logic Analyzer (VLA), SDK/debugger.

This course presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC or MicroBlaze.

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Architect 3

Course duration – 3 days

Price – $2700 or 27 Xilinx Training Credits

Course Part Number – EMBD-33050

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC and/or the MicroBlaze microprocessor.

Prerequisites

- Designing FPGAs Using the Vivado Design Suite 1
- Designing FPGAs Using the Vivado Design Suite 2
- Essentials of Microprocessors
- Basic understanding of C programming
- Basic HDL (VHDL or Verilog) modeling experience

Alternative training

- Embedded Systems Design
- Zynq System Architecture
- Zynq UltraScale+ MPSoC for the System Architect

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

This course has more material than can be covered in three days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student interest. In addition, two of the labs are longer labs that cover several aspects of embedded design in one lab.

Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1: Extended student/Instructor demonstration and follow along lab:** Investigate AXI bus, AXI interconnect, DMA performance, and tips and tricks of Vivado Logic Analyzer. Benchmark DMA performance. Understand relationship between settings in IP Integrator and SDK drivers/headers/APIs.

Day 2

- Formal Introduction to AXI
- Zynq All Programmable SoC PS-PL interface
- Programable SoC
- Zynq All Programmable SoC Booting
- Zynq All Programmable SoC Memory resources
- **Lab 2**: Debugging on the Zynq All Programmable SoC

Day 3

- Meeting Performance Goals
- Embedded Design Overview
- IP and the PS Configuration Wizard
- **Lab 3**: Extended student/Instructor Demonstration and follow along lab. Integrating a simple, highly illustrative piece of IP into AXI, with cross functional troubleshooting. Troubleshoot using SDK, Vivado XSIM, Vivado Logic Analyzer, and/or digital oscilloscope. Custom VHDL and lab instructions included
- Optional (if time permits): constructing and using a Finite Impulse Reponse DSP subsystem with data movers, including software drivers.

In addition to the above, you will receive the following printed materials and labs that can be done after class:

SS Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- **Lab 1:** Building a Zynq All Programmable SoC Platform
- Processor Input/Output Peripherals
- Introduction to AXI
- Zynq All Programmable SoC PS-PL Interface
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC
- Zynq All Programmable SoC Booting
- **Lab 3:** Using DMA on the Zynq All Programmable SoC

SS Day 2

- Zynq All Programmable SoC Memory Resources
- Meeting Performance Goals
- **Lab 4:** Impact of Port Selection on System Performance
- Zynq All Programmable SoC Hardware Design

- Zynq All Programmable SoC Software Design
- Debugging the Zynq All Programmable SoC
- **Lab 5:** Debugging on the Zynq All Programmable SoC
- Zynq All Programmable SoC Tools and Reference Designs
- **Lab 6:** Running and Debugging a Linux Application on the Zynq All Programmable SoC

SS Day 3

- Embedded UltraFast Design Methodology {Lecture, Demo}
- Overview of Embedded Hardware Development {Lecture, Demo}
- Driving the IP Integrator Tool {Lecture, Lab}
- Overview of Embedded Software Development {Lecture}
- Driving the SDK Tool {Lecture, Lab}
- AXI: Introduction {Lecture}
- AXI: Variations {Lecture}
- AXI: Transactions {Lecture, Lab, Demo}
- Introduction to Interrupts {Lecture}
- Interrupts: Hardware Architecture and Support {Lecture}

SS Day 4

- AXI: Connecting AXI IP {Lecture, Demo}
- Using the Create and Import Wizard to Create a New AXI IP {Lecture, Lab}
- AXI: BFM Simulation Using Verification IP (Lecture, Lab}
- MicroBlaze Processor Architecture Overview {Lecture, Lab}
- MicroBlaze Processor Block Memory Usage {Lecture}
- Zynq-7000 All Programmable SoC Architecture Overview {Lecture, Lab, Demo}
- Zynq UltraScale+ MPSoC Architecture Overview {Lecture, Lab, Demo}

Lab Descriptions

- **SS Lab 1:** Building a Zynq All Programmable SoC Platform – Examine the process of using the Vivado IP Integrator tool to create a simple processing system.
- **SS Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **SS Lab 3:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **SS Lab 4:** Impact of Port Selection on System Performance – Explore bandwidth issues surrounding the use of the Accelerator Coherency Port (ACP) and the High Performance (HP) ports.
- **SS Lab 5:** Debugging on the Zynq All Programmable SoC – Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.
- **SS Lab 6:** Running and Debugging a Linux Application on the Zynq All Programmable SoC – Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.
- **SS Lab 7:** Driving the IP Integrator Tool: This lab walks you through all the capabilities of the Vivado® IP integrator tool.
- **SS Lab 8:** Driving the SDK Tool: This lab introduces you to the basic operations for SDK. Concepts such as project creation, adding existing source code to an application, compilation and linking, and downloading are covered. Numerous other labs focus on other aspects of the SDK tools.
- **SS Lab 9:** AXI: Transactions: AXI4 transactions will be explored in this lab with special emphasis on AXI channels, handshaking, and the most useful signal members within the AXI interface. The AXI Traffic Generator (ATG) IP example design will serve as the basis of this lab. Simulation of the design will provide the sample AXI traffic to be studied.
- **SS Lab 10:** Using the Create and Import Wizard to Create a New AXI IP: This lab guides you through the process of creating and adding a custom AXI peripheral to the Vivado® IP catalog by using the Create and Package IP Wizard.
- **SS Lab 11:** AXI: BFM Simulation Using Verification IP: This lab illustrates how to build a simulation model and testbench using the VIP in Master mode to generate AXI traffic to a custom peripheral.
- **SS Lab 12:** MicroBlaze Processor Architecture: The student will learn how to instantiate and configure the MicroBlaze processor and use Designer Assistance to complete a design.
- **SS Lab 13:** Zynq-7000 All Programmable SoC Architecture Overview: This introduction to the basic process of instantiating and customizing the processor system (PS) of the Zynq®-7000 All Programmable SoC family of parts illustrates the process of customizing the PS.
- **SS Lab 14:** Zynq UltraScale+ MPSoC Architecture Overview: This introduction to the basic process of instantiating and customizing the processor system (PS) of the Zynq® UltraScale+™ MPSoC family of parts illustrates the process of customizing the PS.

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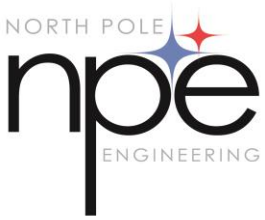

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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