Advanced SDSoC Development Environment and Methodology

Embedded 3

EMBD-ADVSDSOC-ILT (v1.0)

Course Specification

Course Description

This two-day course is structured to help designers employ SDSoC™ development environment optimization techniques to create high-performance, accelerated systems. The focus is on optimizing memory access and hardware functions, generating C-callable IP libraries, and creating custom platforms. The course also includes an introduction to the Xilinx reVISION Stack.

Level – Embedded 3

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – EMBD-ADVSDSOC-ILT

Who Should Attend? – Anyone interested in implementing SDSoC development environment optimization techniques.

Prerequisites

- Zynq System Architecture or Zynq Master Training for Experienced FPGA Engineers
- Experience or training on C programming language
- Embedded Systems Software Design
- SDSoC Development Environment and Methodology

Software Tools

- SDx™ development environment 2017.3

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Improve the memory accesses and data transfer rate between the PS and PL (macro-architecture optimization)
- Apply HLS directives to enhance the performance of hardware functions (micro-architecture optimization)
- Create a C-callable library for IP blocks written in a hardware description language like VHDL or Verilog
- Override tool defaults to improve the performance of individual accelerators and the overall system
- Create a custom platform using the SDSoC Platform Utility (sdspfm)
- Describe how the reVISION Stack enables users to quickly develop applications based on machine learning and computer vision with the SDx development environment

Course Outline

Day 1

- SDSoC Environment Optimization {Lecture}
- Memory Access Optimization {Lecture, Lab}
- Blocking and Non-Blocking Implementations in the SDSoC Tool {Lecture, Lab}
- Implementing Multiple Accelerators in the SDSoC Tool {Lecture, Lab}
- Basics of the Vivado HLS Tool {Lecture}
- Design Exploration with Directives (Pragmas) {Lecture}
- Pipeline for Performance: PIPELINE {Lecture, Demo, Lab)
- Pipeline for Performance: DATAFLOW {Lecture, Lab)

Day 2

- Optimizing Structures for Performance {Lecture, Demo, Lab}
- C-Callable IP Library {Lecture, Lab}
- SDSoC Platform Creation {Lecture, Lab}
- Optimizing the Design {Lecture, Lab}
- reVISION Stack {Lecture}

Topic Descriptions

- SDSoC Environment Optimization {Lecture} – Describes different optimization techniques in the SDSoC development environment, such as macro-architecture and micro-architecture optimizations.
- Memory Access Optimization {Lecture, Lab} – Describes how to improve the memory access and the data transfer rate between the PS and PL.
- Blocking and Non-Blocking Implementations in the SDSoC Tool {Lecture, Lab} – Addresses how the processor behaves while the accelerator is producing solutions—does it wait or continue on?
- Implementing Multiple Accelerators in the SDSoC Tool {Lecture, Lab} – There are times when moving a single function to hardware is not enough—multiple functions must be moved to hardware, or one accelerator must be duplicated. Here students will learn to control how the tool produces the accelerators.
- Basics of the Vivado HLS Tool {Lecture} – Explore the basics of high-level synthesis and the Vivado HLS tool.
- Design Exploration with Directives (Pragmas) {Lecture} – Explore different optimization techniques that can improve the design performance.
- Pipeline for Performance: PIPELINE {Lecture, Demo, Lab) – Describes the PIPELINE directive for improving the throughput of a design.
- Pipeline for Performance: DATAFLOW {Lecture, Lab) – Describes the DATAFLOW directive for improving the throughput of a design by pipelining the functions to execute as soon as possible.
- Optimizing Structures for Performance {Lecture, Demo, Lab} – Learn the performance limitations caused by arrays in your design. You will also learn some optimization techniques to handle arrays for improving performance.
- C-Callable IP Library {Lecture, Lab} – Describes how to create a C-callable library for IP blocks written in a hardware description language like VHDL or Verilog.
- SDSoC Platform Creation {Lecture, Lab} – Describes how to create a custom SDSoC platform starting from a hardware system built using the Vivado Design Suite, and a software run-time environment, including an operating system kernel, boot loaders, file system, and libraries.
- Optimizing the Design {Lecture, Lab} – Apply all the techniques you have learned to meet the performance goal for a given design.
- reVISION Stack {Lecture} – Describes the Xilinx reVISION Stack and how it enables application developers to quickly develop applications based on machine learning or computer vision using the SDx development environment.

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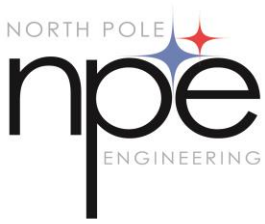

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
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- Student cancellations must be sent here.

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- We regret from time to time classes will need to be rescheduled or cancelled.
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