Embedded Systems Design

Embedded Hardware 3

EMBD-HW-ILT (v1.0)

Course Specification

Course Description

This course is designed to bring FPGA designers up to speed on developing embedded systems using the Vivado® Design Suite. The features and capabilities of both the Zynq® All Programmable System on a Chip (SoC) and the MicroBlaze™ soft processor are covered in lectures, demonstrations, and labs, along with general embedded concepts, tools, and techniques. The hands-on labs provide students with experience designing, expanding, and modifying an embedded system, including adding and simulating a custom AXI-based peripheral.

The Xilinx Zynq All Programmable SoC enables a new level of system design capabilities over previous embedded technologies and this is highlighted throughout the course.

Level – Embedded Hardware 3

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – EMBD-HW-ILT

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx Zynq All Programmable SoC or MicroBlaze soft processor core

Prerequisites

- FPGA design experience
- Completion of the Designing FPGAs Using the Vivado Design Suite 1 course or equivalent knowledge of Xilinx Vivado® software implementation tools recommended
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience (VHDL or Verilog) recommended

Software Tools

- Vivado Design or System Edition 2017.1

Hardware

- Architecture: Zynq-7000 All Programmable SoC (Cortex™-A9 processor) and MicroBlaze processor
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard

* This course focuses on the Zynq-7000 All Programmable SoC architecture. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a MicroBlaze or Cortex-A9 processor using the Vivado IP integrator and Customization Wizard
- Develop software applications utilizing the Eclipse-based Software Development Kit (SDK)
- Create and integrate an IP-based processing system component in the Vivado Design Suite
- Design and add a custom AXI interface-based peripheral to the embedded processing system
- Simulate a custom AXI interface-based peripheral using a bus functional model (BFM)

Course Outline

This course may have more material than can be covered in two days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student interest.

Day 1

- Embedded UltraFast Design Methodology {Lecture, Demo}
- Overview of Embedded Hardware Development {Lecture, Demo}
- Driving the IP Integrator Tool {Lecture, Lab}
- Overview of Embedded Software Development {Lecture}
- Driving the SDK Tool {Lecture, Lab}
- AXI: Introduction {Lecture}
- AXI: Variations {Lecture}
- AXI: Transactions {Lecture, Lab, Demo}
- Introduction to Interrupts {Lecture}
- Interrupts: Hardware Architecture and Support {Lecture}

Day 2

- AXI: Connecting AXI IP {Lecture, Demo}
- Using the Create and Import Wizard to Create a New AXI IP {Lecture, Lab}
- AXI: BFM Simulation Using Verification IP (Lecture, Lab}
- MicroBlaze Processor Architecture Overview {Lecture, Lab}
- MicroBlaze Processor Block Memory Usage {Lecture}
- Zynq-7000 All Programmable SoC Architecture Overview {Lecture, Lab, Demo}
- Zynq UltraScale+ MPSoC Architecture Overview {Lecture, Lab, Demo}

Topic Descriptions

Day 1

- Embedded UltraFast Design Methodology – Outlines the different elements that comprise the Embedded Design Methodology.
- Overview of Embedded Hardware Development – Overview of the embedded hardware development flow.
- Driving the IP Integrator Tool – Describes how to access and effectively use the IPI tool.
- Overview of Embedded Software Development – Reviews the process of building a user application.
- Driving the SDK Tool – Introduces the basic behaviors required to drive the SDK tool to generate a debuggable C/C++ application.
- AXI: Introduction – Introduces the AXI protocol.
- AXI: Variations – Describes the differences and similarities among the three primary AXI variations.
- AXI: Transactions – Describes different types of AXI transactions.
- Introduction to Interrupts – Introduces the concept of interrupts, basic terminology, and generic implementation.
- Interrupts: Hardware Architecture and Support – Reviews the hardware that is typically available to help implement and manage interrupts.

Day 2

- AXI: Connecting AXI IP – Describes the relationships between different types of AXI interfaces and how they can be connected to form hierarchies.
- Using the Create and Import Wizard to Create a New AXI IP – Explains how to use the Create and Import Wizard to create and package an AXI IP.
- AXI: BFM Simulation Using Verification IP – Describes how to perform BFM simulation using the Verification IP.
- MicroBlaze Processor Architecture Overview – Overview of the MicroBlaze microprocessor architecture.
- MicroBlaze Processor Block Memory Usage – Highlights how block RAM can be used with the MicroBlaze processor.
- Zynq-7000 All Programmable SoC Architecture Overview – Overview of the Zynq-7000 All Programmable SoC architecture.
- Zynq UltraScale+ MPSoC Architecture Overview – Overview of the Zynq UltraScale+ MPSoC architecture.

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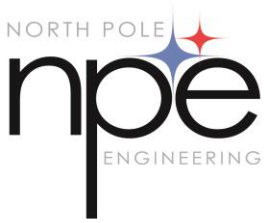

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
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- For additional information or to schedule a private class contact us here.