

Course Description

This one-day course is structured to help designers new to the SDSoC™ development environment to quickly create accelerated systems. The focus is on utilizing the tools to accelerate an existing design at the system architecture level, not on the optimization of the accelerator microarchitectures.

Several optional modules are provided to quickly provide students with the necessary background on both hardware and software. The first half of this class is Level 1 while the afternoon's topics are at Level 2.

Level – Embedded 1 (morning), Embedded 2 (afternoon)

Course Duration – 1 day

Price – \$800 or 8 Xilinx Training Credits

Course Part Number – EMBD-SDSOC-ILT

Who Should Attend? – Anyone interested in quickly adding hardware acceleration to a software system.

Prerequisites

- Understanding of Zynq®-7000 architecture (with emphasis on ACP, HP ports, and internal routing)
- Comfort with the C programming language
- Familiarity with the Vivado® Design Suite, Vivado HLS tool, and Xilinx SDK

Highly Recommend

- [C-based Design: High-Level Synthesis with the Vivado HLx Tool](#)
- [Embedded Systems Software Development](#)

Software Tools

- SDSoC development environment 2016.2

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with [North Pole Engineering, Inc.](#) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify candidate functions for hardware acceleration by using the TCF profiling tool
- Use the System Debugger's capabilities to control the execution flow and examine memory and variables during a debug session
- Move designated software functions to hardware and estimate the performance of the accelerator and the effect on the entire system
- Override tool defaults to improve the performance of the individual accelerators and the overall system

Course Outline

- Zynq AP SoC Architecture Support for Accelerators [Optional]
- Software Overview [Optional]
- SDSoC Tool Overview {Lecture, Two Demos, Lab}
- SDSoC Tool Design Best Practices {Lecture, Demo}
- Application Profiling {Lecture, Demo, Lab}
- Application Debugging {Lecture, Demo, Lab}
- Understanding Estimations in the SDSoC Tool {Lecture, Demo, Lab}
- Blocking and Non-Blocking Implementations in the SDSoC Tool {Lecture, Lab}
- Implementing Multiple Accelerators in the SDSoC Tool {Lecture, Two Labs}
- SDSoC Platform Creation {Lecture, Lab}
- Hardware/Software Event Tracing {Lecture, Lab}

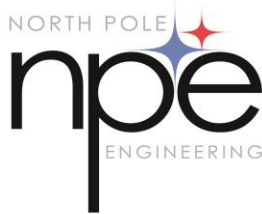
Topic Descriptions

- Zynq AP SoC Architecture Support for Accelerators [Optional] – Discusses the relevant aspects of the Zynq All Programmable SoC architecture for accelerator design. The focus is on AXI ports and protocols, system latency, and memory utilization.
- Software Overview [Optional] – Provides a thorough understanding of how the integrated design environment works, including how the compiler and linker behave, basics of makefiles, DMA usage, and variable scope.
- SDSoC Tool Overview {Lecture, Two Demos, Lab} – Introduces the purpose, underlying structures, and basic functionality of the SDSoC development environment through a combination of lecture and demonstration. Student will cement their knowledge with a lab that reinforces the concepts provided in the lecture and demo.
- SDSoC Design Best Practices {Lecture, Demo} – Illustrates common mistakes and how to avoid them. Also describes approaches to refactoring software for hardware acceleration.
- Application Profiling {Lecture, Demo, Lab} – Profiling is the process that identifies how the processor is spending its time. Through profiling, the user can quickly identify which functions must be optimized or moved to hardware to satisfy the performance requirements.
- Application Debugging {Lecture, Demo, Lab} – Through the use of the System Debugger, students will learn how to follow the control flow in an executing application and see the effects of the code on memory to successfully debug software issues.
- Understanding Estimations in the SDSoC Tool {Lecture, Demo, Lab} – Once a function is moved to hardware, questions remain: Will the accelerator fit in hardware? Will it run fast enough? Estimations can provide the answers.
- Blocking and Non-Blocking Implementations in the SDSoC Tool {Lecture, Lab} – Addresses how the processor behaves while the accelerator is producing solutions—does it wait or continue on?
- Implementing Multiple Accelerators in the SDSoC Tool {Lecture, Lab} – There are times when moving a single function to hardware is not enough—multiple functions must be moved to hardware, or one accelerator must be duplicated. Here students will learn to control how the tool produces the accelerators.
- SDSoC Platform Creation {Lecture, Lab} – Describes how to create a custom SDSoC platform starting from a hardware system built using the Vivado Design Suite, and a software run-time environment, including operating system kernel, boot loaders, file system, and libraries.
- Hardware/Software Event Tracing {Lecture, Lab} – Hardware/software event trace helps the user to understand the performance of their application given the workload, hardware/software partitioning, and system design choices. Such information helps the user to optimize and improve system implementation.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

Visit www.npe-inc.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).