Zynq All Programmable SoC System Architecture

Embedded Architect 3

EMBD-ZSA-ILT (v1.0)

Course Specification

Course Description

The Xilinx Zynq® All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course provides system architects with the knowledge to effectively architect a Zynq All Programmable SoC.

This course presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC.

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Architect 3

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – EMBD-ZSA-ILT

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC.

Prerequisites

- Designing FPGAs Using the Vivado Design Suite 1
- Designing FPGAs Using the Vivado Design Suite 2
- Understanding of C programming
- VHDL or Verilog

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

This course has more material than can be covered in two days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student interest.

Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- **Lab 1:** Building a Zynq All Programmable SoC Platform
- Processor Input/Output Peripherals
- Introduction to AXI
- Zynq All Programmable SoC PS-PL Interface
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC
- Zynq All Programmable SoC Booting
- **Lab 3:** Using DMA on the Zynq All Programmable SoC

Day 2

- Zynq All Programmable SoC Memory Resources
- Meeting Performance Goals
- **Lab 4:** Impact of Port Selection on System Performance
- Zynq All Programmable SoC Hardware Design
- Zynq All Programmable SoC Software Design
- Debugging the Zynq All Programmable SoC
- **Lab 5:** Debugging on the Zynq All Programmable SoC
- Zynq All Programmable SoC Tools and Reference Designs
- **Lab 6:** Running and Debugging a Linux Application on the Zynq All Programmable SoC

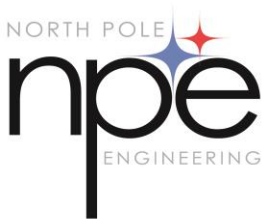
Lab Descriptions

- **Lab 1:** Building a Zynq All Programmable SoC Platform – Examine the process of using the Vivado IP Integrator tool to create a simple processing system.
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **Lab 3:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **Lab 4:** Impact of Port Selection on System Performance – Explore bandwidth issues surrounding the use of the Accelerator Coherency Port (ACP) and the High Performance (HP) ports.
- **Lab 5:** Debugging on the Zynq All Programmable SoC – Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.
- **Lab 6:** Running and Debugging a Linux Application on the Zynq All Programmable SoC – Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

Visit **www.npe-inc.com/training**, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.