

Course Description

This two-day course is structured to provide system architects with an overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family.

Level – Embedded System Architect 3

Course Duration – 2 days

Price – \$1600 or 16 Xilinx Training Credits

Course Part Number – EMBD-ZUPSA-ILT

Who Should Attend? – System architects interested in understanding the capabilities and ecosystem of the Zynq UltraScale+ MPSoC device.

Prerequisites

- Suggested: [Zynq Master Training for experienced FPGA designers.](#)
- Familiarity with embedded operating systems

Software Tools

- Vivado® Design Suite 2017.3
 - May require special Zynq UltraScale+ MPSoC family license
- Hardware emulation environment:
 - VirtualBox
 - QEMU
 - Ubuntu desktop
 - PetaLinux

Hardware

- Host computer for running the above software*

* This course focuses on the Zynq UltraScale+ MPSoC architecture. Check with [North Pole Engineering, Inc.](#) for the specifics of the in-class lab board or other customizations. This version of the class does not use a physical board, but rather a local emulation environment and the Vivado Design Suite.

After completing this comprehensive training, you will have the necessary skills to:

- Effectively use power management strategies and leverage the capabilities of the platform management unit (PMU)
- Identify mechanisms to secure and safely run the system
- Outline the high-level architecture of the devices
- Define the boot sequences appropriate to the needs of the system

Course Outline

Day 1

- Zynq UltraScale+ MPSoC Overview {Lecture, Demo, Lab}
- Zynq UltraScale+ MPSoC HW-SW Virtualization {Lecture, Demo, Lab}
- QEMU {Lecture, Demo, Lab}
- Zynq UltraScale+ MPSoC Security and Software {Lecture, Demo}

Day 2

- Zynq UltraScale+ MPSoC Power Management {Lecture, Demo, Lab}
- Zynq UltraScale+ MPSoC System Coherency {Lecture}
- Zynq UltraScale+ MPSoC DDR and QoS {Lecture, Demo, Lab}
- Zynq UltraScale+ MPSoC Booting {Lecture, Lab}
- Zynq UltraScale+ MPSoC Ecosystem Support {Lecture}

Topic Descriptions

Day 1

- Zynq UltraScale+ MPSoC Overview – Overview of the Zynq UltraScale+ MPSoC device.
- Zynq UltraScale+ MPSoC HW-SW Virtualization – Covers the hardware and software elements of virtualization. The lab demonstrate how hypervisors can be used.
- QEMU – Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available.
- Zynq UltraScale+ MPSoC Security and Software – Defines what safety and security is in the context of embedded systems and introduces several standards.

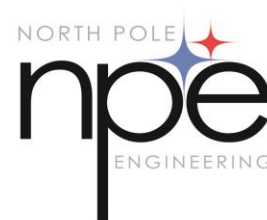
Day 2

- Zynq UltraScale+ MPSoC Power Management – Overview of the PMU and the power-saving features of the device.
- Zynq UltraScale+ MPSoC System Coherency – Learn how information is synchronized within the API and through the ACE/AXI ports.
- Zynq UltraScale+ MPSoC DDR and QoS {Lecture, Demo, Lab} – Understand how DDR can be configured to provide the best performance for your system.
- Zynq UltraScale+ MPSoC Booting – How to implement the embedded system, including the boot process and boot image creation. Also how to detect a failed boot.
- Zynq UltraScale+ MPSoC Ecosystem Support – Overview of supported operating systems, software stacks, hypervisors, etc.

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- Student cancellations must be sent [here](#).

NPE Course Cancellation Policy

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