Vivado Design Suite Advanced XDC and Static Timing Analysis for ISE Software Users

FPGA 2

FPGA-VAXDC4ISE-ILT (v1.0)

Course Specification

Course Description

This course will update experienced FPGA designers to utilize the Vivado® Design Suite. Learn the underlying database and static timing analysis (STA) mechanisms. Utilize Tcl for navigating the design, creating Xilinx design constraints (XDC), and creating timing reports. Learn to make appropriate timing constraints for SDR, DDR, source-synchronous, and system-synchronous interfaces for your FPGA design.

You will also learn to make path-specific, false path, and min/max timing constraints, as well as learn about timing constraint priority in the Vivado timing engine. Finally, you will learn about the scripting environment of the Vivado Design Suite and how to use the project-based scripting flow.

You will also learn the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level – FPGA 2

Course Duration – 3 days

Price – $2400 or 24 Xilinx Training Credits

Course Part Number – FPGA-VAXDC4ISE-ILT

Who Should Attend? – Existing Xilinx ISE Design Suite FPGA designers

Prerequisites

- FPGA design experience
- Advanced knowledge Xilinx ISE or of competing FPGA technology tools.
- Intermediate VHDL or Verilog knowledge

Software Tools

- Vivado Design or System Edition 2017.1

Hardware

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and 7 series architectures. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Access primary objects from the design database and filter lists of objects using properties
- Describe setup and hold checks and describe the components of a timing report
- Create appropriate input and output delay constraints and describe timing reports that involve input and output paths
- Explain the impact that manufacturing process variations have on timing analysis and describe how min/max timing analysis information is conveyed in a timing report
- Describe all of the options available with the `report_timing` and `report_timing_summary` commands
- Describe the timing constraints required to constrain system-synchronous and source-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Create scripts for the project-based and non-project batch design flows
- Describe the UltraFast design methodology checklist
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experience

Course Outline

Day 1

- UltraFast Design Methodology: Design Closure {Lecture}
- UltraFast Design Methodology: Advanced Techniques {Lecture}
- Timing Constraints Wizard {Lecture, Lab}
- Timing Constraint Editor {Lecture}
- Introduction to Vivado Reports {Lecture, Demo}
- Introduction to Clock Constraints {Lecture, Lab, Demo}
- Report Clock Interaction {Lecture, Demo}
- Report Clock Networks {Lecture, Demo}
- I/O Constraints and Virtual Clocks {Lecture, Lab}
- Timing Summary Report {Lecture, Demo}
- Setup and Hold Timing Analysis {Lecture}
- Generated Clocks {Lecture, Demo}
- Clock Group Constraints {Lecture, Demo}
- Introduction to Timing Exceptions {Lecture, Lab, Demo}

Day 2

- Synchronization Circuits {Lecture, Lab, Case Study}
- Report Datasheet {Lecture, Demo}
- Baselining {Lecture, Lab, Demo}
- Pipelining {Lecture, Lab}
- I/O Timing Scenarios {Lecture}
- Source-Synchronous I/O Timing {Lecture, Lab}
- System-Synchronous I/O Timing {Lecture, Demo}
- Timing Constraints Priority {Lecture}
- Case Analysis {Lecture}
- Introduction to Floorplanning {Lecture}
- Physical Optimization {Lecture, Lab}

Topic Descriptions

Day 1

- UltraFast Design Methodology: Design Closure – Introduces the UltraFast™ methodology guidelines on design closure.
- UltraFast Design Methodology: Advanced Techniques – Introduces the methodology guidelines for advanced techniques.
- Timing Constraints Wizard – Use the Timing Constraints Wizard to apply missing timing constraints in a design.
- Timing Constraints Editor – Introduces the timing constraints editor tool to create timing constraints.
- Introduction to Vivado Reports – Generate and use Vivado timing reports to analyze failed timing paths.
- Introduction to Clock Constraints – Apply clock constraints and perform timing analysis.
- Report Clock Interaction – Use the clock interaction report to identify interactions between clock domains.

- Report Clock Networks – Use report clock networks to view the primary and generated clocks in a design.
- I/O Constraints and Virtual Clocks – Apply I/O constraints and perform timing analysis.
- Timing Summary Report – Use the post-implementation timing summary report to sign-off criteria for timing closure.
- Setup and Hold Timing Analysis – Understand setup and hold timing analysis.
- Generated Clocks – Use the report clock networks report to determine if there are any generated clocks in a design.
- Clock Group Constraints – Apply clock group constraints for asynchronous clock domains.
- Introduction to Timing Exceptions – Introduces timing exception constraints and applying them to fine tune design timing.

Day 2

- Synchronization Circuits – Use synchronization circuits for clock domain crossings.
- Report Datasheet – Use the datasheet report to find the optimal setup and hold margin for an I/O interface.
- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Pipelining – Use pipelining to improve design performance.
- I/O Timing Scenarios – Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.
- Source-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.
- System-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.
- Timing Constraints Priority – Identify the priority of timing constraints.
- Case Analysis – Understand how to analyze timing when using multiplexed clocks in a design.
- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks while floorplanning.
- Physical Optimization – Use physical optimization techniques for timing closure.

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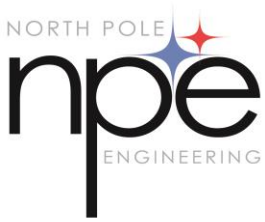

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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