VHDL and Advanced VHDL using Vivado Design Suite

FPGA 1

FPGA-VHDLADVVHDLVDS-ILT (v1.0)

Course Specification

Course Description

This comprehensive two-part course is a thorough introduction to the VHDL language using Vivado Design Suite. The emphasis during the first three days is on writing solid synthesizable code and enough simulation code to write a viable testbench with techniques aimed at creating parameterizable and reusable designs. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically using the Vivado Design Suite. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. In this five-day course, you will gain valuable hands-on experience designing FPGAs using the Vivado Design Suite. Incoming students with little or no VHDL knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

During the second stage of this course, Increase your VHDL proficiency by learning advanced techniques that will help you write more robust and reusable code. This comprehensive course is targeted toward designers who already have some experience with VHDL.

The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs as compared to lecture modules.

Level – FPGA 1

Course Duration – 5 days

Price – $4000 or 40 Xilinx Training Credits

Course Part Number – FPGA-VHDLADVVHDLVDS-ILT

Who Should Attend? – Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs while learning important aspects of the Vivado Design Suite 2017.1 tool.

Prerequisites

- Basic digital design knowledge (BSEE or BSCE recommended)
- This is a challenging course delivered at a fast pace.

Alternative training

- Designing with VHDL
- Advanced VHDL

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 or Kintex-7 FPGA KC705 board*

* This course does not focus on any particular architecture. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information
- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines [FSMs], RAM/ROM data structures)
- Simulate a basic VHDL design
- Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
- Optimize VHDL code to target specific silicon resources within the Xilinx FPGA
- Create and manage designs within the Vivado Design Suite environment

Course Outline

This condensed course provides more material to the student than can be covered in five days. The focus is on learning and using VHDL to design FPGAs and write testbenches while also learning the Vivado Design Suite. All slides and lab instructions will be provided to students. However, this course also contains real world labs without detailed written instructions, in which engineers apply what they learn while thinking and working in a team environment, under the guidance of the instructor, in a more real-world project. Many features of the Vivado Design Suite are also covered. All of the detailed labs are also available for self-study, and these labs are useful for future review if an engineer doesn't get utilize all of the topics covered in this class for a period of weeks or months after the class completes.

COURSE AGENDA IS TENATIVE AT THIS POINT

Day 1

- Vivado Design Suite Language Templates
- Xilinx documentation on synthesis constructs
- Data types and what it means to be strongly typed
- Concurrent Operations
- Processes and variables
- **Lab 1:** Designing a Simple Process
- Testbenches for simulation
- Vivado Simulator Basics
- **Lab 2:** Simulating a Simple Design

Day 2

- Testbenches for synthesis
- Writing a synthesizable testbench for vector code coverage
- Vivado Logic Analyzer (VLA) and Virtual Input Output (VIO)
- **Long Lab 3**: VectorGenerator of DUT with output checker in using VLA and VIO

Day 3

- Loops and Conditional Elaboration
- **Lab 4:** Using Loops
- Writing a synthesizable testbench for vector code coverage
- Vivado Logic Analyzer (VLA) and Virtual Input Output (VIO)
- Enumerated Types and State machines (one, two, and three process)
- **Long lab 5**: State machine
- Attributes: built-in and vendor defined

Day 4

- Functions and Procedures
- Packages and Libraries in the Vivado Design Suite

- Records

Day 5

- Multiple architectures for a single entity
- Mapping architectures via configuration files in the Vivado Design Suite
- Attributes: built-in and vendor defined
- Functions and Procedures
- Packages and Libraries in the Vivado Design Suite

SS Day 1

- The "Shape" of VHDL
- Demo: Multiplexer
- **Lab 1:** Using the Tools
- Data Types
- Concurrent Operations
- **Lab 2:** Using Concurrent Statements
- Processes and Variables
- **Lab 3:** Designing a Simple Process

SS Day 2

- Introduction to Testbenches
- Vivado Simulator Basics
- **Lab 4:** Simulating a Simple Design
- Creating Memory
- **Lab 5:** Building a Dual-Port Memory
- Finite State Machines
- **Lab 6:** Building a Moore Finite State Machine
- Targeting Xilinx FPGAs
- **Lab 7:** Xilinx Tool Flow

SS Day 3

- Loops and Conditional Elaboration
- **Lab 8:** Using Loops
- Attributes
- Functions and Procedures
- Packages and Libraries
- **Lab 9:** Building Your Own Package
- Interacting with the Simulation
- Writing a Good Testbench
- **Lab 10:** Building a Meaningful Testbench

SS Day 4

- VHDL Overview
- Simulation Concepts
- Advanced Data Types
- Subprograms and Design Attributes
- **Lab 11:** Flexible Functions
- Access Type Techniques and Blocks
- **Lab 12:** Linked Lists with Access Types
- Utilizing File IO
- **Lab 13:** TextIO Techniques

SS Day 5

- Advanced Techniques in VHDL
- **Lab 14:** Creating Real-World Simulations
- Supporting Multiple Platforms
- **Lab 15:** Supporting Multiple Platforms
- Non-Integer Numbers
- **Lab 16:** Implementing Fixed and Floating Point Numbers
- Appendix: Guarded Signals

Lab Descriptions

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. You will write, synthesize, simulate, and implement all the labs. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits.

Register Today

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