

Course Description

This comprehensive course is a thorough introduction to the Verilog language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall Verilog proficiency and enhance your FPGA optimization. This course covers Verilog 1995 and 2001.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no Verilog knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

Level – FPGA 1

Course Duration – 3 days

Price – \$2400 or 24 Xilinx training Credits

Course Part Number – LANG-VERILOG-ILT

Who Should Attend? – Engineers who want to use Verilog effectively for modeling, design, and synthesis of digital designs

Prerequisites

- Basic digital design knowledge

Follow-up training

- [Designing with SystemVerilog](#)
- [Verification with SystemVerilog](#)

Alternative training

- [Designing with Verilog and SystemVerilog](#)

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 or Kintex-7 FPGA KC705 board*

* This course does not focus on any particular architecture. Check with [North Pole Engineering, Inc.](#) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize Xilinx FPGAs by using Verilog
- Use enhanced Verilog file I/O capability
- Run a timing simulation by using Xilinx Simprim libraries
- Create and manage designs within the Vivado Design Suite environment
- Download to the evaluation demo board

Course Outline

This course may have more material than can be covered in three days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student consensus.

Day 1

- Introduction to Verilog {Lecture}

- Verilog Keywords and Identifiers {Lecture}
- Verilog Data Values and Number Representation {Lecture}
- Verilog Data Types {Lecture}
- Verilog Buses and Arrays {Lecture}
- Verilog Modules and Ports {Lecture, Lab, Demo}
- Verilog Operators {Lecture}
- Continuous Assignment {Lecture}
- Gate-Level Modeling {Lecture}
- Procedural Assignment {Lecture}
- Blocking and Non-Blocking Procedural Assignment {Lecture, Lab}
- Procedural Timing Control {Lecture}

Day 2

- Verilog Conditional Statements: if_else {Lecture, Lab}
- Verilog Conditional Statements: case {Lecture}
- Verilog Loop Statements {Lecture}
- Introduction to Verilog Testbenches {Lecture, Lab}
- System Tasks {Lecture}
- Verilog Sub-Programs {Lecture}
- Verilog Functions {Lecture}
- Verilog Tasks {Lecture}
- Verilog Compiler Directives {Lecture}
- Verilog Parameters {Lecture, Lab}
- Verilog Generate Statement {Lecture}

Day 3

- Verilog Timing Checks {Lecture}
- Finite State Machines {Lecture}
- Mealy Finite State Machine {Lecture, Lab}
- Moore Finite State Machine {Lecture, Lab}
- FSM Coding Guidelines {Lecture}
- File I/O: Introduction {Lecture}
- File I/O: Read Functions {Lecture, Lab}
- File I/O: Write Functions {Lecture}
- Targeting Xilinx FPGAs {Lecture, Lab}
- User-Defined Primitives {Lecture}
- Programming Language Interface {Lecture}

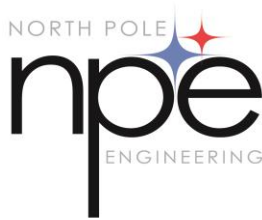
Lab Descriptions

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. The labs are written, synthesized, behaviorally simulated, and implemented by the student. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that students verify in simulation.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
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