Designing with VHDL

FPGA 1

LANG-VHDL-ILT (v1.0)

Course Specification

Course Description

This comprehensive course is a thorough introduction to the VHDL language using Vivado Design Suite. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn best coding practices that will increase your overall VHDL proficiency and prepare you for the Advanced VHDL course.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no VHDL knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

Level – FPGA 1

Course Duration – 3 days

Price – $2400 or 24 Xilinx Training Credits

Course Part Number – LANG-VHDL-ILT

Who Should Attend? – Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs while learning basics of Vivado Design Suite 2017.1

Prerequisites

- Basic digital design knowledge (BSEE or BSCE recommended)

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 or Kintex-7 FPGA KC705 board*

* This course does not focus on any particular architecture. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information
- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines [FSMs], RAM/ROM data structures)
- Simulate a basic VHDL design
- Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
- Optimize VHDL code to target specific silicon resources within the Xilinx FPGA
- Create and manage designs within the Vivado Design Suite environment

Course Outline

This course has more material than can be covered in three days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student interest.

Day 1

- The "Shape" of VHDL
- Demo: Multiplexer
- **Lab 1:** Using the Tools
- Data Types
- Concurrent Operations
- **Lab 2:** Using Concurrent Statements
- Processes and Variables
- **Lab 3:** Designing a Simple Process

Day 2

- Introduction to Testbenches
- Vivado Simulator Basics
- **Lab 4:** Simulating a Simple Design
- Creating Memory
- **Lab 5:** Building a Dual-Port Memory
- Finite State Machines
- **Lab 6:** Building a Moore Finite State Machine
- Targeting Xilinx FPGAs
- **Lab 7:** Xilinx Tool Flow

Day 3

- Loops and Conditional Elaboration
- **Lab 8:** Using Loops
- Attributes
- Functions and Procedures
- Packages and Libraries
- **Lab 9:** Building Your Own Package
- Interacting with the Simulation
- Writing a Good Testbench
- **Lab 10:** Building a Meaningful Testbench

Lab Descriptions

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. You will write, synthesize, simulate, and implement all the labs. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

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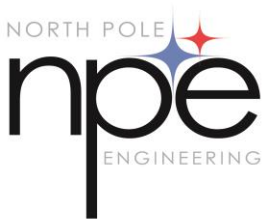

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.